



Molecular Crystals and Liquid Crystals

Publication details, including instructions for authors and subscription information:

<http://www.tandfonline.com/loi/gmcl20>

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Version of record first published: 22 Sep 2010

To cite this article: M. Yoshida, K. Suemori, S. Uemura, S. Hoshino, T. Kodzasa, T. Kamata, T. Kondo, H. Kawai & T. Kawai (2007): Highly Sensitive Organic Photo-FET Using Photosensitive Polymer Insulator, *Molecular Crystals and Liquid Crystals*, 471:1, 21-27

To link to this article: <http://dx.doi.org/10.1080/15421400701544489>

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We fabricated a photo field effect transistor (photo FET) having a poly (N-vinyl carbazole) (PVK) insulator layer. PVK was employed as a photosensitive insulator material for the Photo FET. In this photo FET, illumination of a blue light to the PVK insulator drastically improved the field effect mobility and the gate-switching ratio. This result would be due to that the photo-generated carriers in the PVK layer were effectively accumulated in the gate capacitor of the photo FET.

Keywords: gate dielectric; OFET; pentacene; photo-transistor; PVK

INTRODUCTION

Organic Field Effect Transistors (OFETs) have been noticed as a possible candidate for next-generation electronic devices for recent years [1–3]. Since there are many kinds of organic materials, they can give various special functions to OFETs [4, 5]. Especially, we have paid attention to and investigated polymeric gate insulators employed

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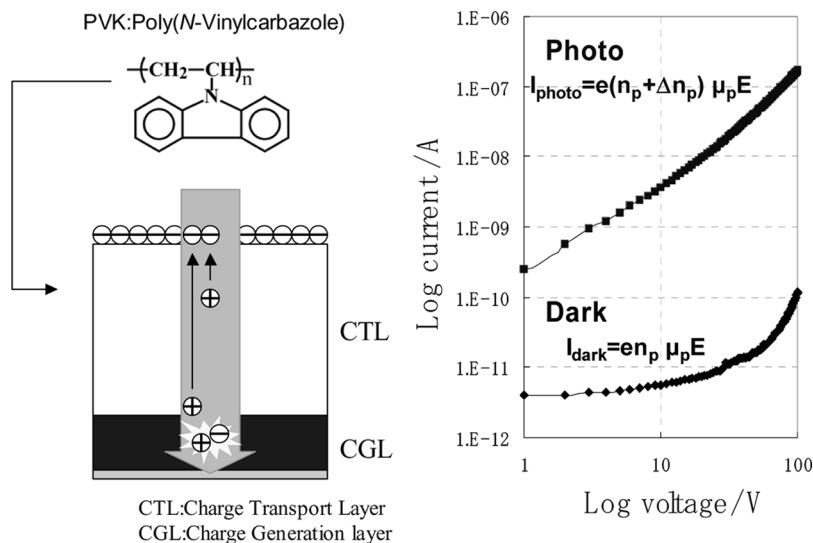


FIGURE 1 Chemical structure of poly(*N*-vinylcarbazole) (PVK) and photoconductivity of PVK.

in the part of the OFETs. Some sorts of polymeric materials, utilized as photosensitizing drums in laser printers or photocopiers, have photoconductive properties as shown in Figure 1 [6]. Therefore, they

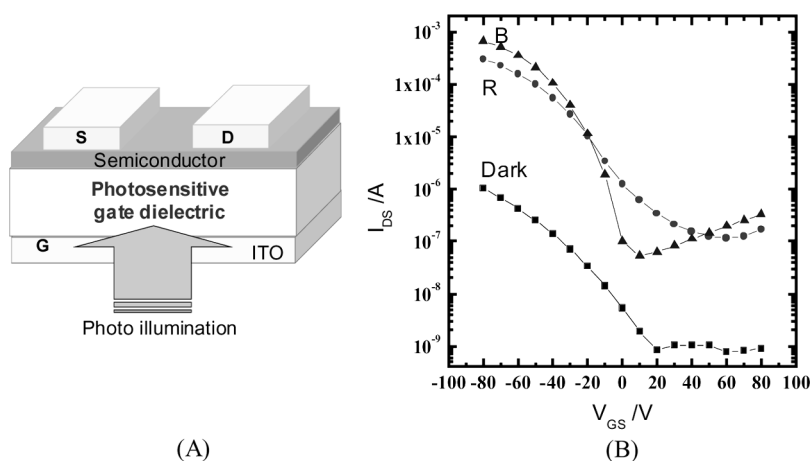


FIGURE 2 (A) and (B). Schematic diagram of the PhotoFET structure (A). Transfer characteristics for the pentacene FET having the PVK insulator layer under dark and photo-illumination conditions (B).

work as insulators in dark condition and as conductors in photo-illumination condition, reversibly. By using their photoconductive properties, we have intent to add photo-switching and photo-memory functions to OFETs. For example, poly(N-vinylcarbazole) (PVK) has been known as a good photoconductor [6]. Further, the PVK has high processability and high durability to applied voltage, therefore, this is expected to work as a good gate insulator for OFETs in dark condition. For the purpose of giving photofunctions to OFETs, we have fabricated a pentacene FET having a PVK insulator (Fig. 2(A)), and we have been especially interested in transistor behavior of the OFET on illuminating the PVK insulator by lights with different wavelengths.

EXPERIMENTAL

Figure 2(A) shows the cross-sectional illustration of our newly developed photo-FET structure that was fabricated as following procedure. An Indium Tin Oxide (ITO) glass was employed as a substrate and a transparent gate electrode. ITO glasses were carefully cleaned before the fabrication of FET devices. A PVK film was cast on the ITO glass from 0.33 wt.% chloroform solution as a photo-sensitive gate insulator. For sensitizing the PVK film to visible light, 2,4,7-trinitro-9-fluorenone (TNF) was doped to the PVK film. Thickness of the cast PVK film resulted in ca. 1.5 μm . A pentacene film (50 nm) was deposited onto the PVK film. Pentacene was train-sublimated 5 times for purification. After that, Au DS electrodes were deposited through the patterned metal mask (channel width W: 5 mm, channel length L: 20 μm). All thin film depositions are carried out by using thermal evaporation method at a pressure of ca. 10^{-6} Torr (deposition rate = 0.1 ~ 0.2 nm/s). Electrical measurements were carried out by using two sourcemeters (Keithley 6430 + 2420). For illuminating the FETs, LEDs were employed (Red (635 nm, Sloan SL905RC); Blue (430 nm, Sloan SL905BCU)). For observing photo-switching behaviors, the PVK insulator was illuminated from the ITO glass side. Gate capacitance of the FET device was measured by LCR meter (Agilent precision impedance analyzer 4294A).

RESULTS AND DISCUSSION

Figure 2(B) shows Transfer characteristics for the pentacene FET having the PVK insulator layer under dark and photo-illumination (R and B) conditions. Under photo-illumination conditions, ON currents are 2 orders of magnitude higher than the ON current under dark condition.

TABLE 1 Field Effect Mobility μ_{FET} , Threshold Voltage V_{th} and ON-OFF Ratios for the Photo-FET Under Illuminating and Dark Conditions

	Dark	Red (635 nm)	Blue (430 nm)
Field effect mobility μ_{FET} (cm^2/Vs)	0.02	1.02	1.94
Threshold voltage V_{th} (V)	24.0	12.4	1.1
ON-OFF ratio*	204	240	6814

*Off currents are I_{DS} values at zero gate bias.

In the case of illumination with B light, drain-source current (I_{DS}) is increasing steeper in the sub-threshold region than the case of dark and R light illumination conditions. Illumination with R light increases ON and OFF current simultaneously, therefore, ON-OFF ratio tends to be decreased drastically. On the contrary, it is notable that illumination with B light practically does not increase OFF current; therefore, ON-OFF ratio is kept high. Since clear saturation of I_{DS} is observed under illumination with B light, adequate hole accumulation would occur in the channel region even at relative low gate voltage. Table 1 shows calculated field effect mobilities μ_{FET} , threshold voltages V_{th} and ON-OFF ratios for the FET under photo-illuminations (R and B) and dark conditions. Calculations of μ_{FET} were carried out by using the following equation

$$\mu_{\text{FET}} = \frac{2LI_{\text{D}}}{WC(V_{\text{G}} - V_{\text{th}})^2} \quad (1)$$

where L is the channel length $20\text{ }\mu\text{m}$, W is the channel width 5 mm , C is capacitance per unit area of PVK layer measured for the Au/pentacene/PVK/ITO MIS structure. As shown in Table 1, under photo-illumination conditions, μ_{FET} are 2 orders of magnitude higher than that under dark condition. It is also remarkable that illumination with B light drastically decreases threshold voltage V_{th} from 24.0 V to 1.1 V and increases the ON-OFF ratio from 204 (dark) to 6814 (blue). As a result, illumination with B light improves the transistor properties substantially. The reason of this improvement of transistor properties can be considered as follows.

In the positive V_{GS} regime, I_{GS} and I_{DS} components mix with each other as shown in Figures 3(A) and (B). Therefore, the measured I_{DS} increases with the increase of positive V_{GS} in the positive direction. In this regime, holes are not accumulated at the channel region and then a conductive channel is not generated, therefore, I_{channel} hardly flow. Namely, the observed I_{DS} is substantially composed of I_{GS} and I_{bulk} . From this fact, subtracting I_{GS} from measured I_{DS} gives I_{bulk}

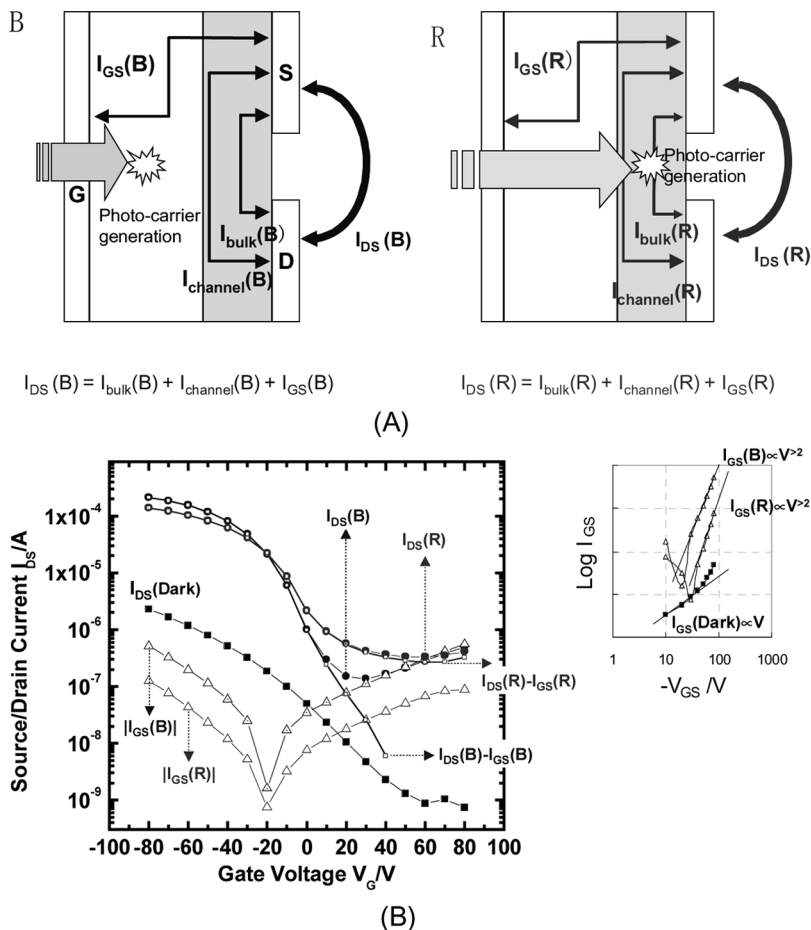


FIGURE 3 (A) and (B). Schematic diagram of current components flowing through the photo-FET under illumination conditions (A) and measured I_{DS} and each current component vs. applied gate voltage (B).

in positive V_{GS} regime (Fig. 4(A)). This result are shown in Figure 4(B) as $I_{bulk} = I_{DS} - I_{GS}$. The difference between $I_{bulk}(R)$ and $I_{bulk}(B)$ shows that R light is absorbed and induces photo-carrier generation in the pentacene bulk. In other word, $I_{bulk}(R)$ is mainly composed of photocurrent by R-light illumination. The bulk photo-carrier generation does not depend on the gate voltage, therefore, that occurs in whole V_{GS} regime. This photocurrent component ($I_{bulk}(R)$) is a main cause of the large off-current for R-light illumination condition.

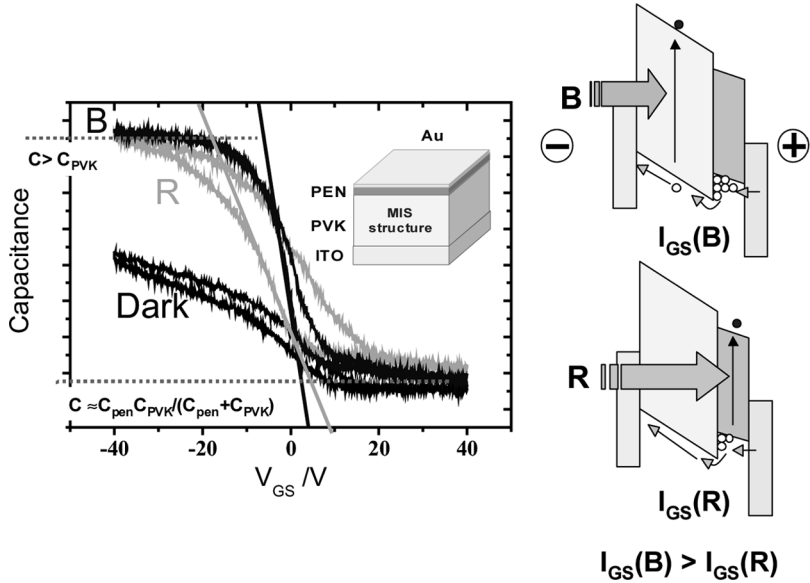


FIGURE 4 CV curves for different illumination conditions and schematic diagrams corresponding to each condition.

On the other hand, B-light illumination does not induce large off-current, because B-light is not absorbed in the pentacene layer but in the PVK layer. Here, we have to consider the reason why B-light illumination improves the transistor properties drastically. At first, we considered that the efficiency of charge accumulation at the conductive channel was improved by B-light illumination, because the sub-threshold slope of $I_{DS}(B)$ became steeper than R-light illumination and dark conditions as shown in Figure 3(B). For the purpose of understanding the charge accumulation process well, the gate-source currents I_{GS} were analyzed in detail in Figure 3(B). Since $I_{GS}(R)$ and $I_{GS}(B)$ are proportional to about $V_{GS}^{>2}$ in the negative V_{GS} regime (Fig. 3(B)), the photo-generated carriers must be related to charge accumulations. $I_{GS}(\text{Dark})$ is proportional to V_{GS} even in negative V_{GS} regime, in this case charge carriers do not form space charge layer in this device. Ohmic $I_{GS}(\text{Dark})$ is not enough large to saturate the channel in this V_{GS} regime. As far as considering the energy diagram of ITO/PVK/Pentacene/Au structure, the PVK/Pentacene interface is most probable place to accumulate the charges.

Figure 4 show CV curves of the ITO/PVK/Pentacene/Au MIS structure under illumination and dark conditions. In the case of

R- and B-light illumination conditions clear saturation behaviors of capacitance are observed in both positive and negative V_{GS} regimes. Under the B-light illumination condition the lowest V_{GS} needs to saturate the capacitor in the negative V_{GS} regime. Namely, hole accumulation occurs most effectively by the B-light illumination because $I_{GS}(B)$ is larger than $I_{GS}(R)$, therefore enough hole carriers to saturate the channel capacitor are provided rapidly. On the other hand, the capacitor cannot completely saturate under the dark condition because the number of holes is too small to do that. Hysteresis properties are observed especially in the curve of R-light illumination condition. This would be because the R-light illumination induces photo-carrier generation in the pentacene bulk and then the generated electrons are trapped to deep trapping sites presented in pentacene bulk.

CONCLUSION

We have developed the novel photo FET using PVK as a photo-sensitive gate dielectric. It has been revealed that illumination with B light absorbed in PVK layer drastically improves transistor properties.

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